a plurality of modules for optimizing a network of a number of the logic structures using placement based information to create an accurate model of the electronic design thereby enabling optimized design information associated with the accurate model to be passed to gate-level implementation tools to achieve predictable results at gate-level implementation of the electronic design.

92

36. (New) The computer program product of claim 35, wherein the performance data for each implementation quantifies a relationship between a timing delay and an output load of the implementation.

37. (New) The computer program product of claim 35, wherein the performance data includes performance data variations for combinations of topology, implementation type, bit width, output driver size, and output load.

REMARKS

Applicant is hereby adding claims 3-37. Favorable action is solicited.

Respectfully submitted,
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Dated: July 31, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Paragraph [0001]:

[0001] This application is a continuation of U.S. Patent Application No. 09/634,927, filed August 8, 2000, now U.S. Patent Number 6,360, 356, which is a continuation of U. S. Patent Application No. 09/015,602, filed January 30, 1998, now U.S. Patent Number 6,145,117.